SUNY POLYTECHNIC INSTITUTE

Cost-Competitive, High-Performance, Highly Reliable Power Devices on Silicon Carbide and Gallium Nitride

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2020 DOE Annual Merit Review

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Project ID # elt247

Overview

Timeline

- Project start April 2019
- Project end March 2024
- Percent Complete: 20%

Budget

- BP1 total $333K: Federal $ 300K + cost share (10%)

Barriers

- Cost: the lack of device innovation s and processing technologies
- Performance: need state-of-the-art facility for tight design rules
- Reliability and ruggedness: trade off relationship with performance

Partners

- Sandia National Laboratories
- The Ohio State University

Relevance - background

Background

- SiC devices have been in the market for several years but they are not ready for insertion in automotive power trains meeting stringent reliability requirements;
- In its zeal to reduce device cost, SiC vendors have sacrificed reliability for lower cost;
- There have been too much stress on the device static performances such as on-resistance, breakdown voltage, and trade-off between them;
- SiC exclusive processes (e.g. ion implants at elevated temperatures) have been adopted without criticism;
- Feedback on dynamic behaviors and circuit level evaluations are not reflected in the device / process designs;
- There are many more aspects to improve in device design, process, packaging and others.

Relevance – objectives / impact

Overall objectives in this project

- The primary objective of this project is to ensure that the next-generation of wide-bandgap devices of sufficient performance, reliability, and price to achieve the system-level DOE goals.

Objectives in previous period (BP1, FY2019-2020)

- Establishment of the process baseline for Gen1 MOSFETs;
- Static performances of Gen1 MOSFETs evaluated: BV=1500V, Ron,sp=6mohm-cm^2, Vth=2V.

Objectives in this period (BP2, FY2020-2021)

- Establishment of the process baseline for Gen2 MOSFETs;
- Static performances of Gen1 MOSFETs evaluated: BV=1600V, Ron,sp=5mohm-cm^2, Vth=2V, Short Circuit SOA 2µs.

Impact of research

- The successful development of the proposed device will bring in a highly efficient and reliable power electronics for electric drive trains.

Milestones – BP1

Milestone	Type	Description
Gen1 SiC MOSFET design	Technical	The cell and edge termination structures for MOSFETs and JBS diode integrated MOSFETs have been optimized ; Optimized devices included in a single mask-set.
Gen1 SiC MOSFETs fabrication	Technical	Two engineering lots to make Gen1 devices completed.
Gen1 SiC MOSFETs evaluation	Technical	Static performances have been characterized on-wafer.
AlGaN/GaN on sapphire	Technical	Optimized devices are grown on Sapphire substrate. State-of-the-art characteristics is shown on-wafer.
Go/No Go Decision: Establishment of the process baseline for Gen1 MOSFETs	Go/No Go	Performances of Gen1 SiC MOSFETs evaluated: BV = 1500V, $R_{on,sp}$= 6 mohm-cm^2, V_{th} = 2V.

Milestones – BP2

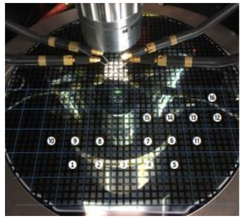
Milestone	Type	Description
Gen2 SiC MOSFET Design	Technical	The cell and edge termination structures for MOSFETs and JBS diode integrated MOSFETs have been optimized; Optimized devices included in a single mask-set.
Gen2 SiC MOSFETs Fabrication	Technical	Two engineering lots to make Gen2 devices completed; Implants conducted at RT; Self-aligned channel scheme developed.
Gen2 SiC MOSFETs Evaluation	Technical	Static performances have been characterized on-wafer.
AlGaN/GaN HEMT growth on HVPE GaN	Technical	Device structures with optimized layer thickness and composition are grown on HVPE GaN
Cost effective process baseline for Gen2 MO SFETs	Go/No Go	Performances of Gen2 SiC MOSFETs evaluated: BV = 1600V, $R_{on,sp}$ = 5 mohm-cm^2, V_{th} = 2V Short Circuit SOA 2µs.

Approach – Leveraging previous and current projects

Demonstration of 1.2kV accumulation / inversion channel SiC MOSFETs

2016

Development of highly efficient edge terminatio n techniques for 3.3kV and 4.5kV SiC devices



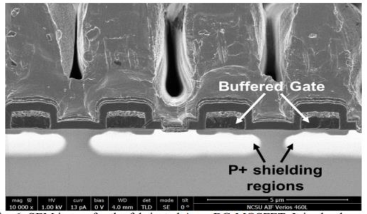
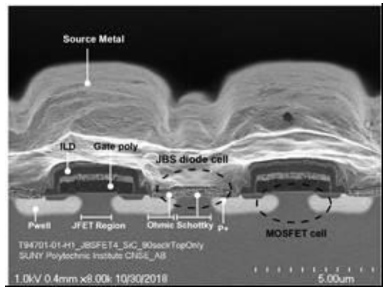


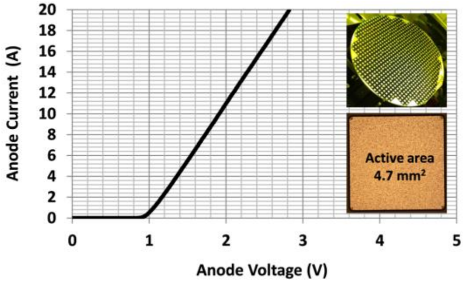
Fig. 6: SEM image for the fabricated Accu BG-MOSFET. It is clearly seen that the split poly-Si gates are buffered by the P+ shielding regions.

High frequency 1.2kV SiC MOSFETs

2017

JBSFET (JBS diode integrated MOSFET)

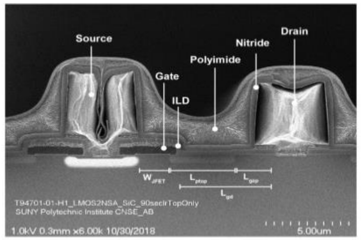


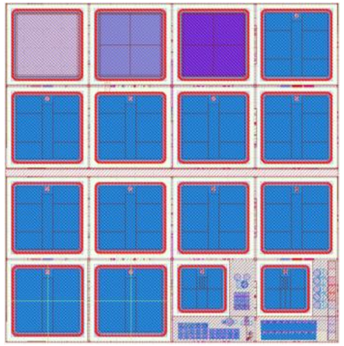


1.7kV SiC JBS diode

2018

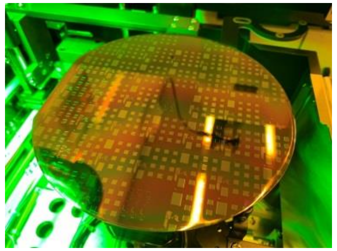
600V Lateral, Vertical MOSFETs / 6.5kV, 10kV SiC MO SFETs





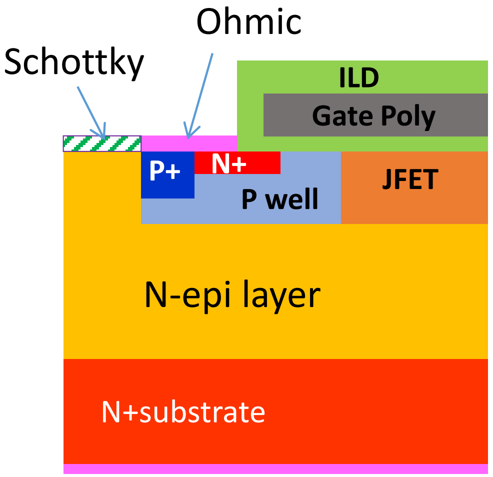
2019

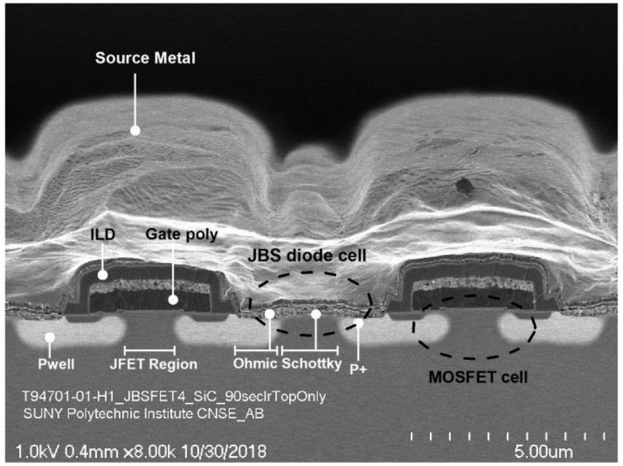
13kV SiC MOSFETs (Army Research Lab.)



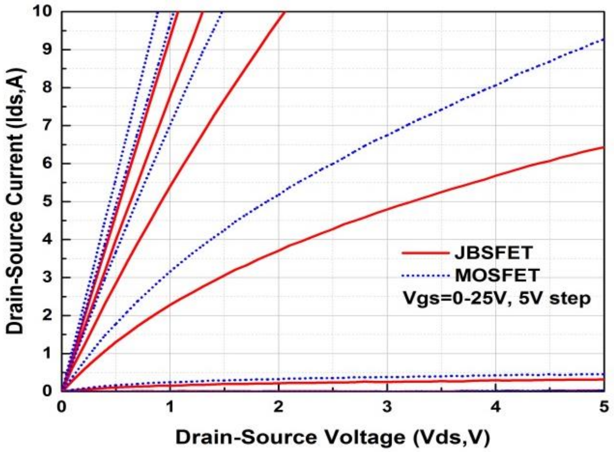
Approach

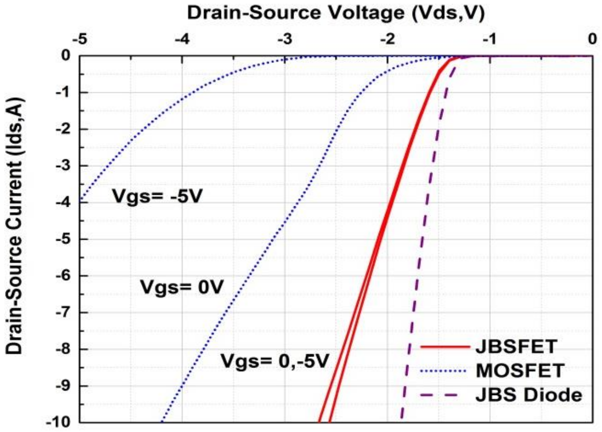
JBSFET (diode integrated MOSFET) as a good example of design innovation

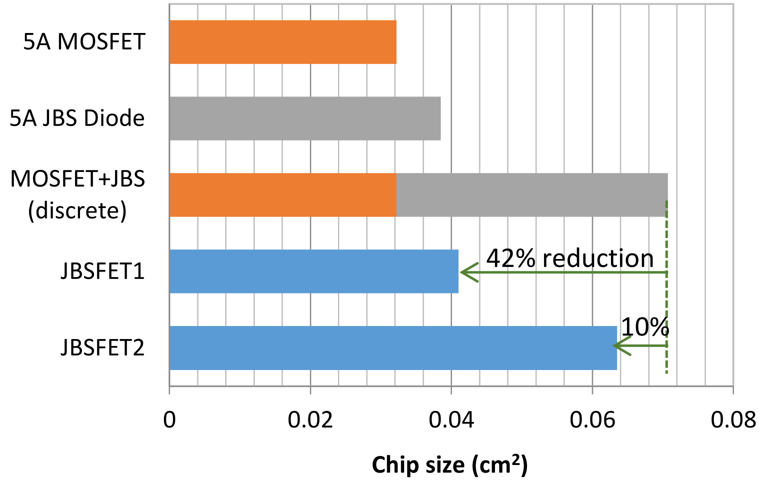




- ~50% save in wafer area – direct reduction in the chip price;
- Free from concerns on BPD induced degradation;
- Reduction in parasitic inductance in package.







Woongje Sung and B. J. Baliga, "On Developing One-Chip Integration of 1.2 kV SiC MOSFET and JBS Diode (JBSFET)," IEEE Transaction on Industrial Electronics, vol.64, no.10, pp. 8206-8212, Oct. 2017

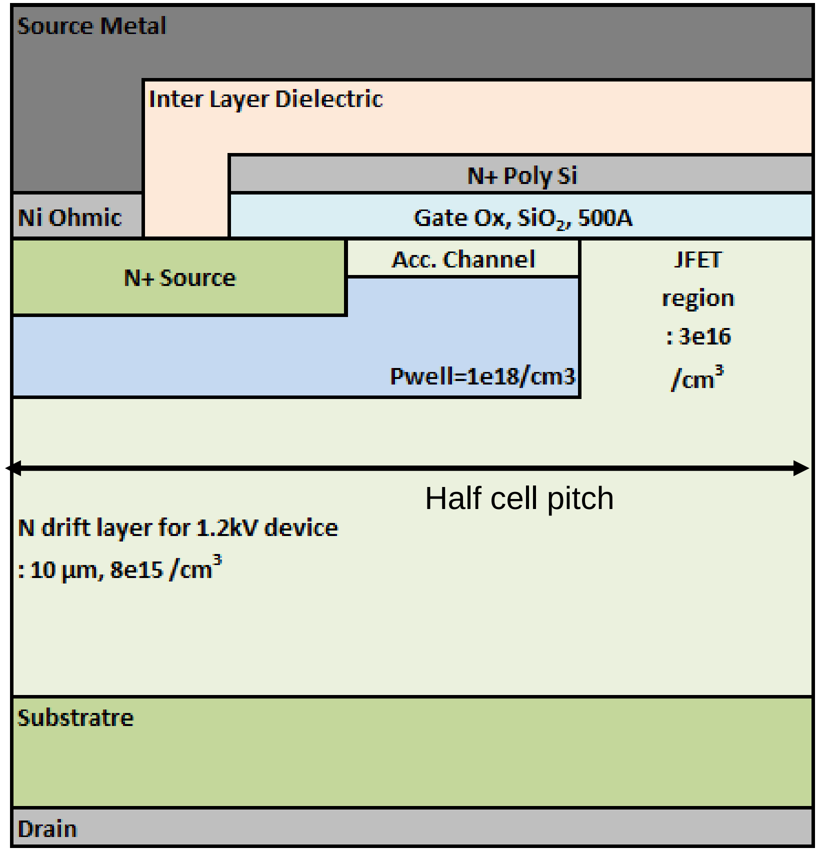
Nick Yun, Justin Lynch, and Woongje Sung, “Area Efficient, 600V 4H-SiC JBS Diode Integrated MOSFETs (JBSFETs) for Power Converter Applications,” IEEE Journal of Emerging and Selected Topics in Power Electronics, Accepted for Publication, Early Access is available (Oct. 15, 2019); 10.1109/JESTPE.2019.2947284.

Approach – CPR metrics

	on-resistance	chip price	blocking behavior	threshold voltage	short circuit capability	avalanche capability	HTRB	HTGB, Vth stability	dv/dt, switching behavior	BPD, SF- degradation	thermal management	others
short channel	+	+	-	-	-		-	-				
tight cell pitch	+	+			-							
self aligned channel	+	+	+	+				+				
narrow JFET region			+		+	+	+		+			
enhanced doping in JFET	+				-	-	-					
deep Pwell (so is JFET region)			+		+	+	+					
thinner gate oxide	+			-	-		-	-				
innovative gate oxide process	+	+		+	+			?		+		
unipolar diode integration		+							+	+		
inversion mode channel	-	-	+	+	+			+				
source doping reduction	-				+							
reduction in Wp+/Wn+	+	+			-	-						
Ringe based edge termination		-	-			-	-		+			
JTE based edge termination		+	+			+	+		-			
substrate thinning	+										+	
double sided package									+		+	
Ion implants @ RT		+								?		
W plug(high aspect ratio CT)	+										+	+
Striped cell design	-		+		+		+				+	

Technical Accomplishments and Progress

- **MOSFET cell optimization**



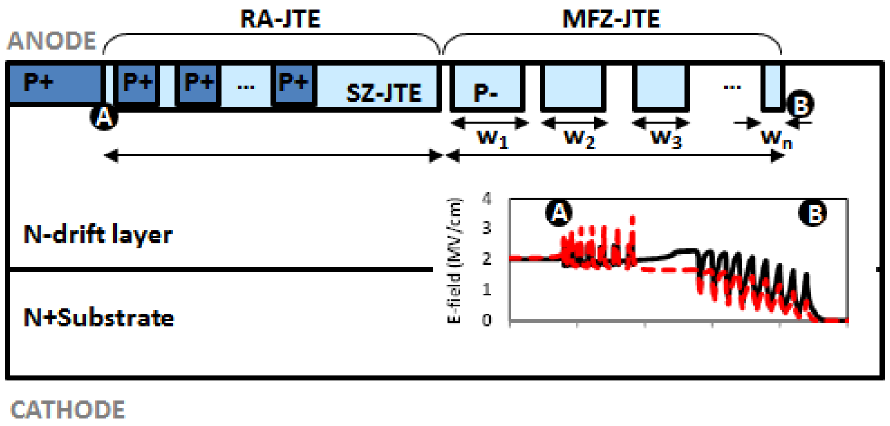
- **Drift layer is designed to achieve approximately 1.7kV;**
- **The cell pitch largely affect R_{on}:**
  -> P+ source is located in the orthogonal direction, intermittently;
  -> short channel is preferred;
- **A higher channel mobility also contribute much to the R_{on}: An accumulation channel is designed;**
- **Design of the JFET region is very important.**

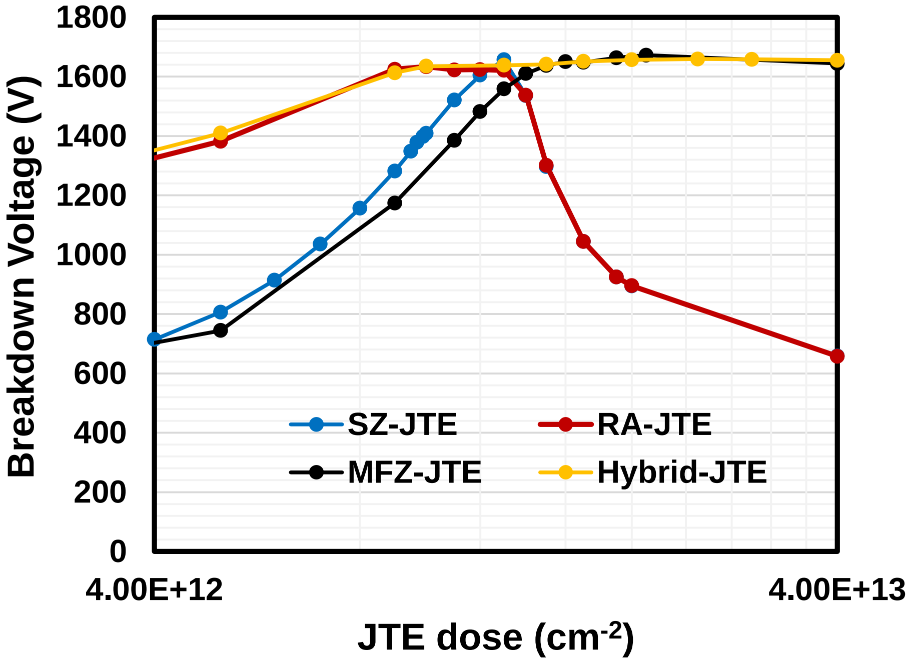
Woongje Sung, Kijeong Han, and B. J. Baliga, "*A comparative study of channel designs for SiC MOSFETs: accumulation mode channel vs. inversion mode channel*," 29th International Symposium on Power Semiconductor Devices and IC's (ISPSD), 2017, **DOI:** 10.23919/ISPSD.2017.7988996

Woongje Sung, Kijeong Han, and B. J. Baliga, "Optimization of the JFET region of 1.2kV SiC MOSFETs for improved high frequency figure of merit (HF-FOM)," IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), 2017, **DOI:** 10.1109/WiPDA.2017.8170553

Technical Accomplishments and Progress

- **Edge termination design**
  - **Hybrid-JTE - simulation**



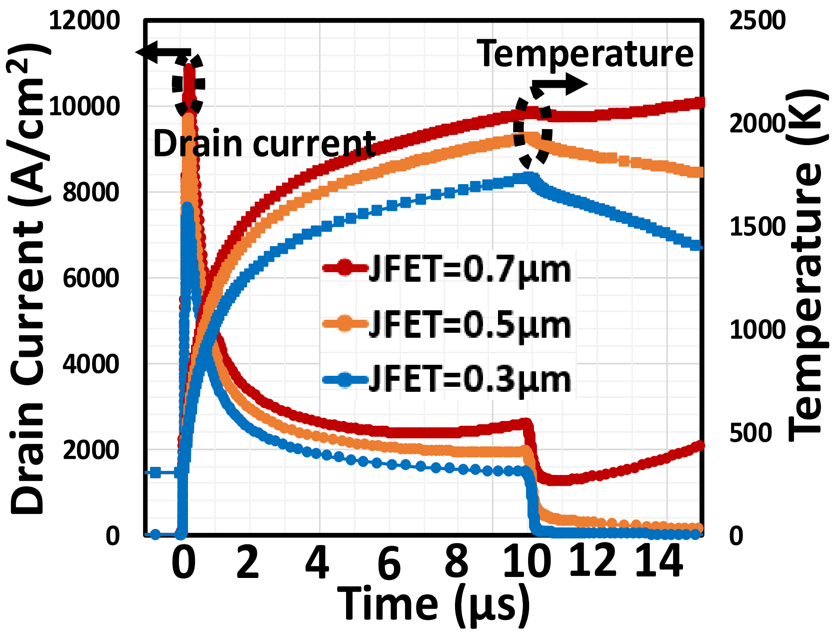


- Hybrid-JTE is combination of RA-JTE and MFZ-JTE;
- Superposition of BVs of RA-JTE and MFZ-JTE results in BVs of the Hybrid-JTE;
- Very wide range of the JTE dose for high BVs is achieved by the Hybrid-JTE;

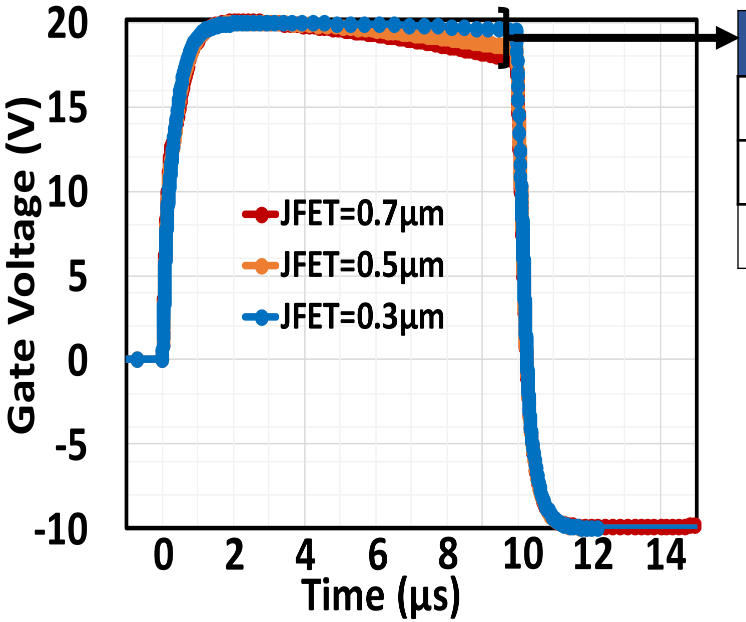
Woongje Sung and B. J. Baliga, “A Near Ideal Edge Termination Technique for 4500V 4H-SiC Devices: the Hybrid Junction Termination Extension (Hybrid-JTE),’’ IEEE Electron Device Lett., vol. 37, no.12, pp. 1609-1612, Dec. 2016. DOI: 10.1109/LED.2016.2623423

Technical Accomplishments and Progress

- **Non-Isothermal simulation – Narrow JFET width**



Simulated drain current and maximum junction temperature in SiC



W_{JFET} (µm)	t_{sc} (µs)
0.7	6.8
0.5	8.2
0.3	13.7

Applied gate voltage from +20 to -10 V during SC event

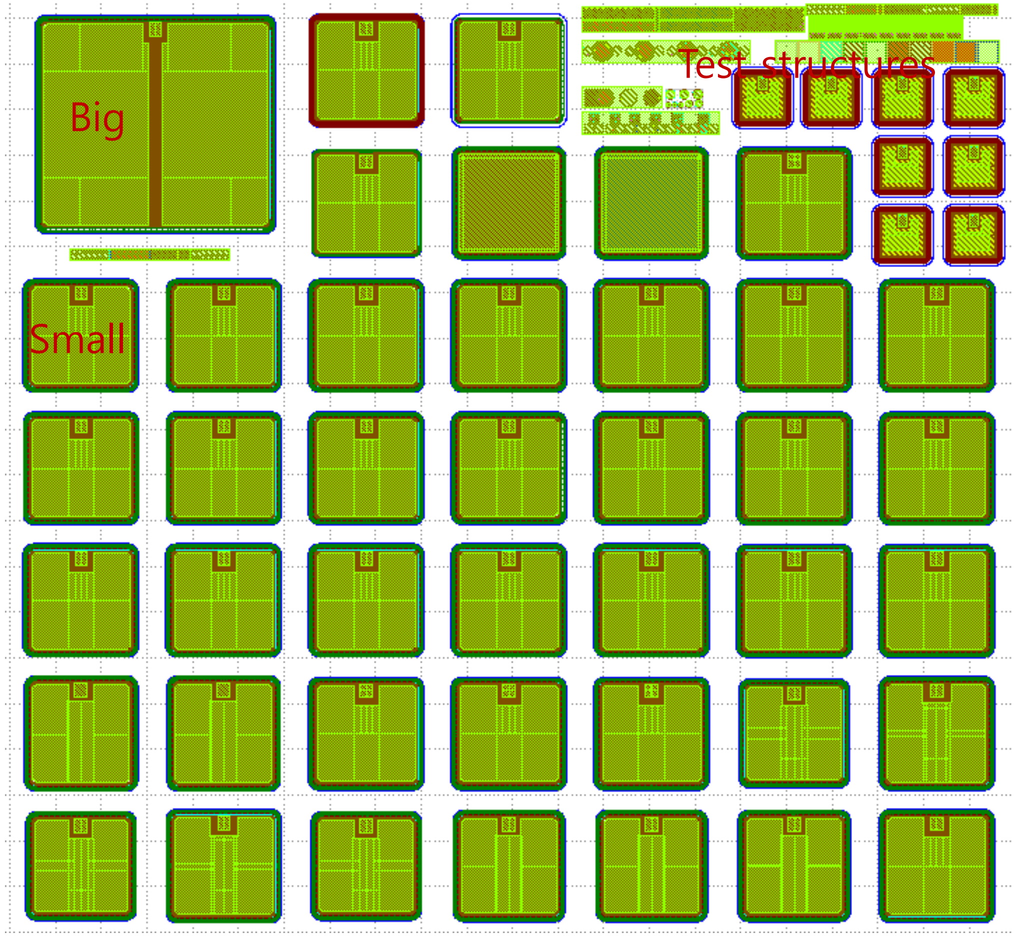
- Mixed-mode simulation with thermode was developed to investigate SC;
- For exact simulation results, Non-Isothermal simulation models were developed;
- Various device structures were evaluated using non-Isothermal simulation.

Dongyoung Kim, Adam Morgan, Nick Yun, Woongje Sung, Anant Agarwal, and Robert Kaplar, "Optimization of Processing and Design of SiC MOSFETs to Enhance Short Circuit Safe Operating Area (SCSOA) on the Basis of Non-Iso Thermal Device Simulations," Accepted for presentation at International Reliability Physics Symposium (IRPS 2020)

Technical Accomplishments and Progress

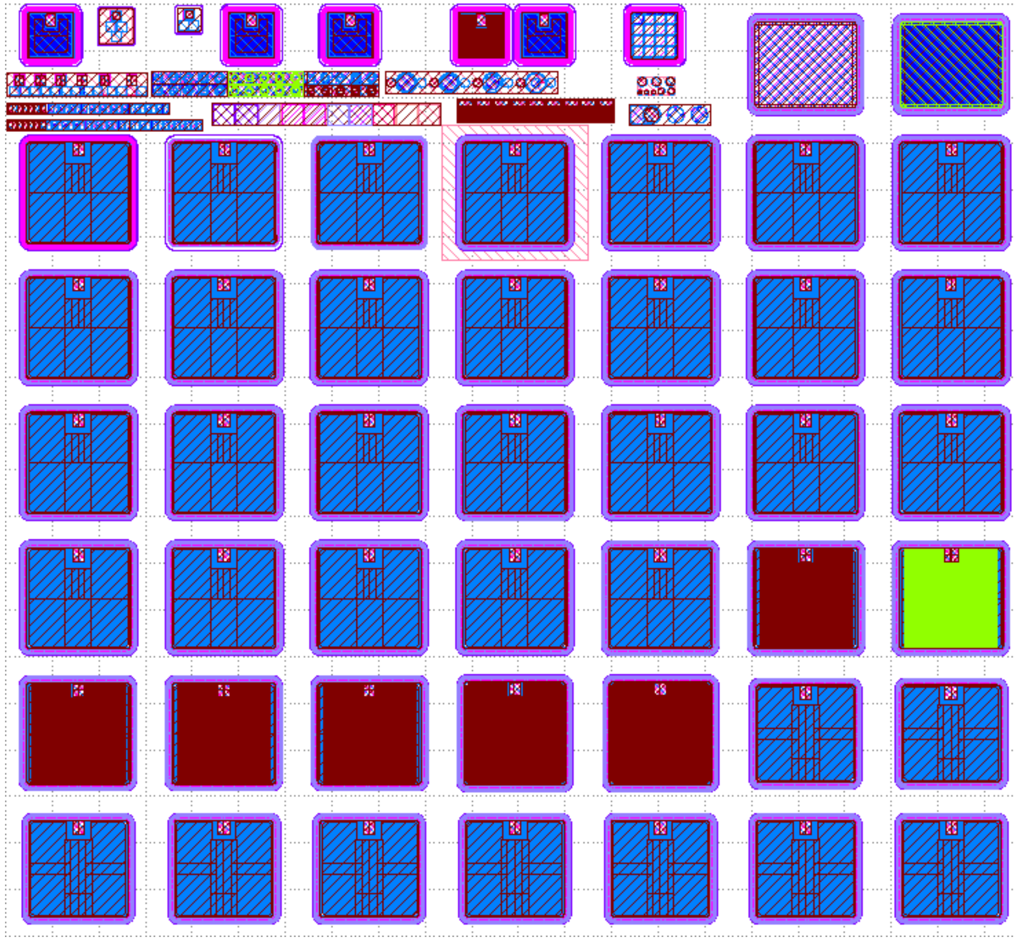
- **Mask design – floor plan for 1st lot**
  - PiN diode, JBS diode, MOSFETs (different sizes), JBSFETs and test structures were included (total 42 different device designs)
  - Design variations:
    - Channel length
    - JFET region width
    - Cell pitch
  - Process split:
    - Pwell depth
    - JFET implant depth
    - Thinner gate oxide
    - Implant temperature

Small device: active ~ 4.5 mm^2
Big devices: active ~ 21 mm^2



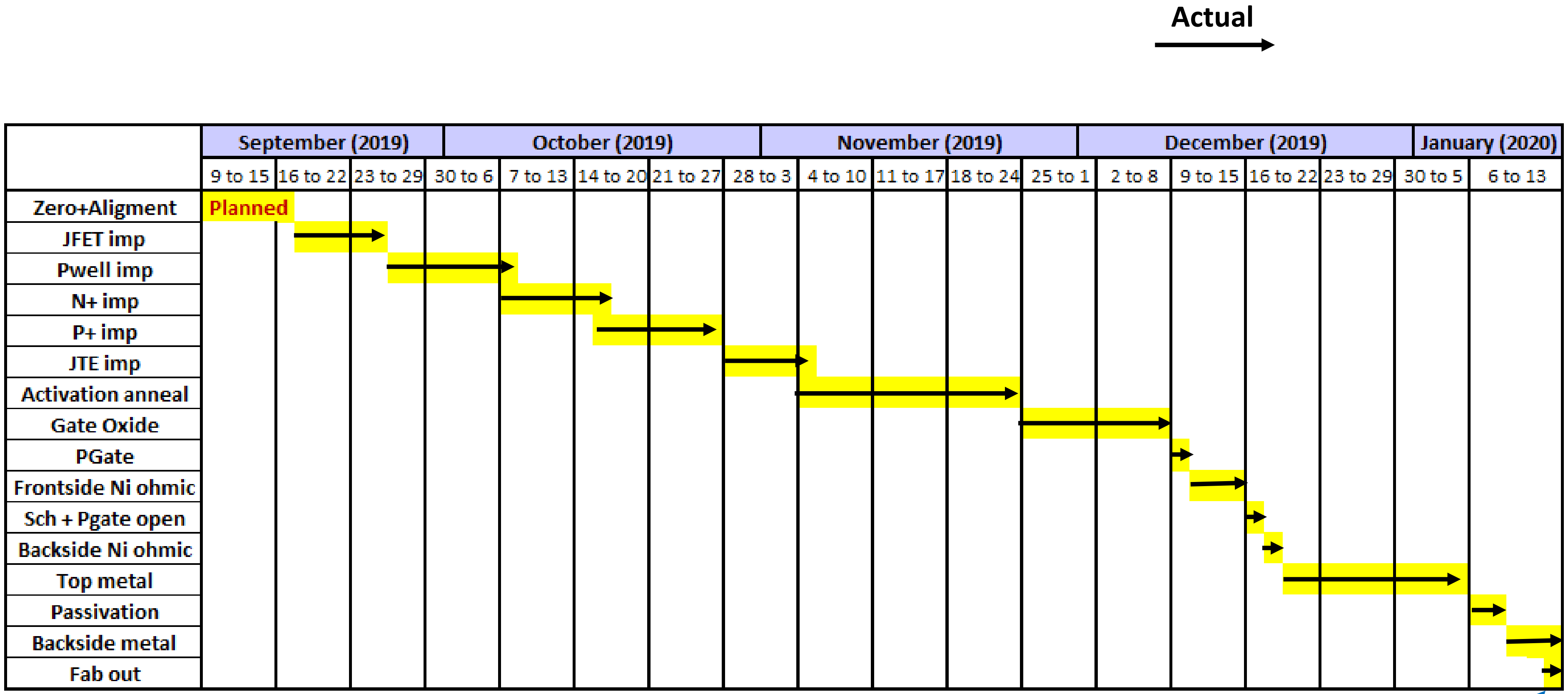
Technical Accomplishments and Progress

- **Mask design – floor plan for 2nd lot**
  - PiN diode, JBS diode, MOSFETs (different sizes), JBSFETs and test structures were included (total 42 different device designs)
  - Design variations:
    - JFET region width
    - Cell pitch
    - Hexagonal layout
  - Process split:
    - Self-aligned channel
    - Doping in the JFET region
    - Channel spreading layer



Technical Accomplishments and Progress

- **Lot1 status**

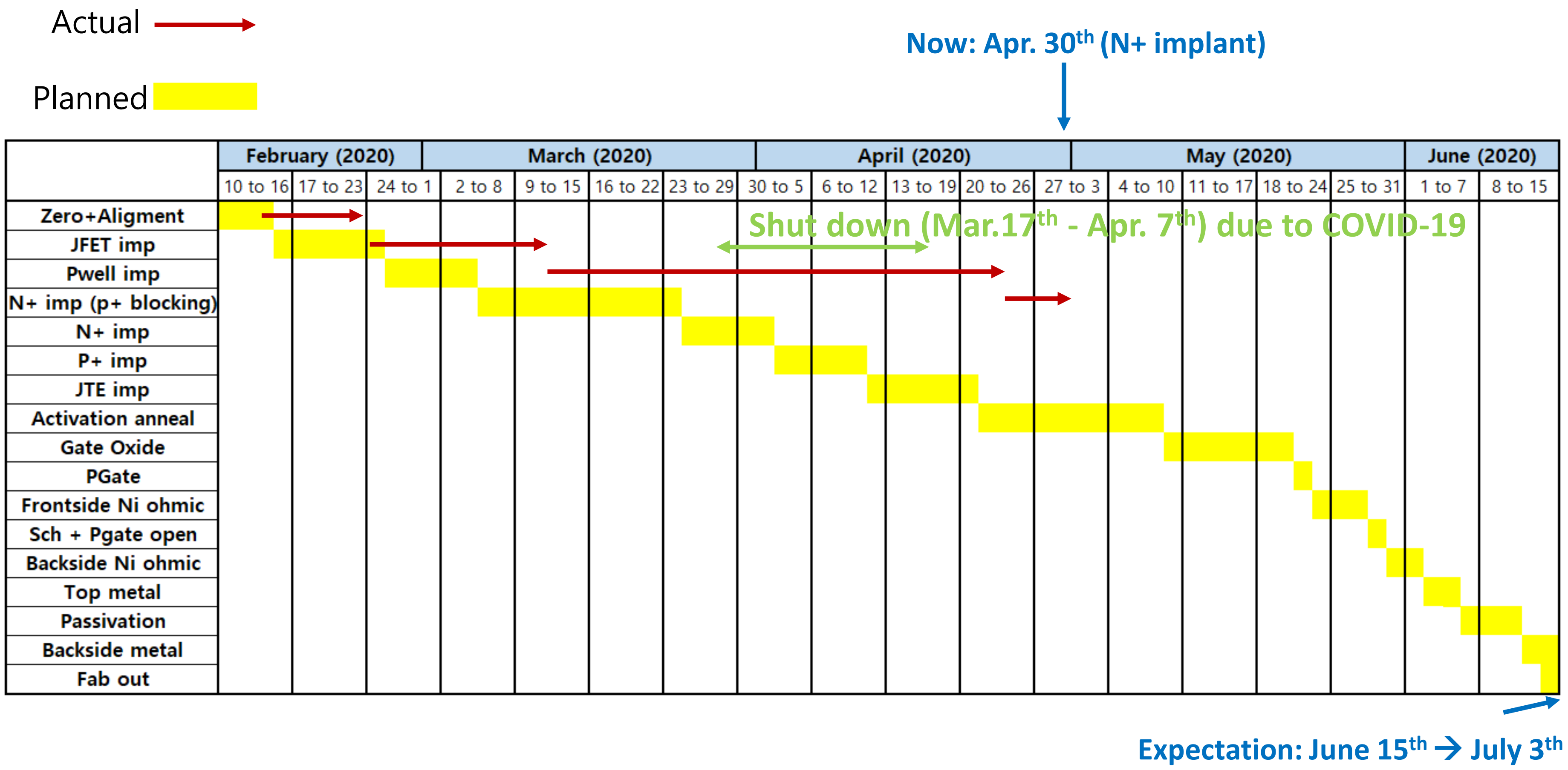


Expectation: Jan. 13th

Now: completed

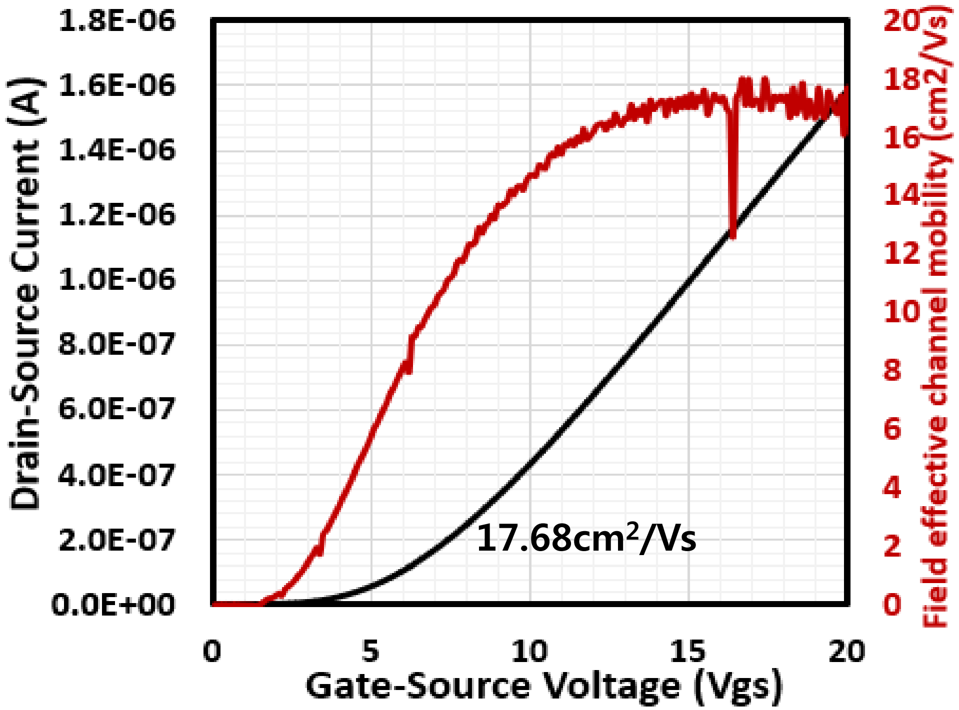
Technical Accomplishments and Progress

- **Lot2 status**

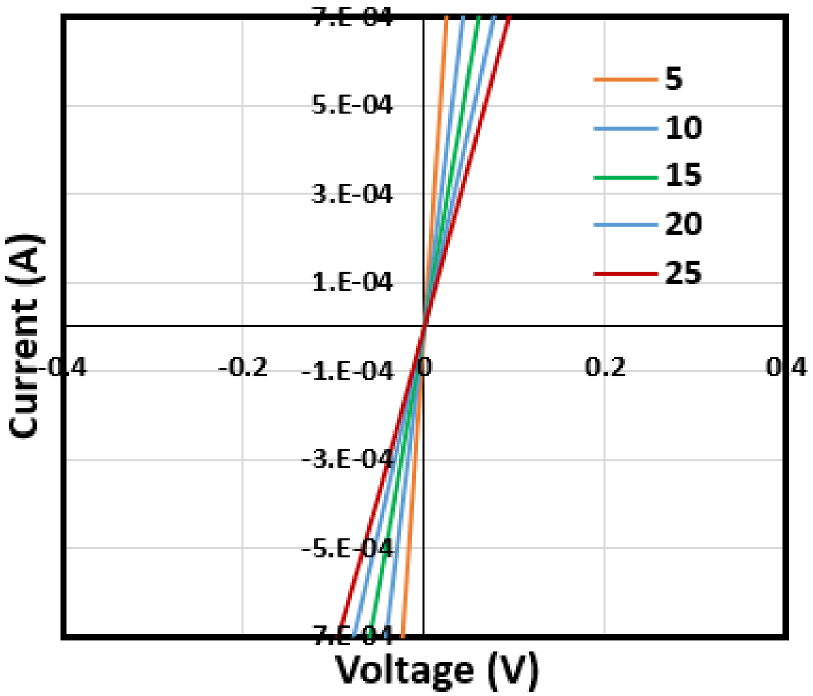


Technical Accomplishments and Progress

- **Lot1 evaluation: channel mobility and contact resistance**



Wf3



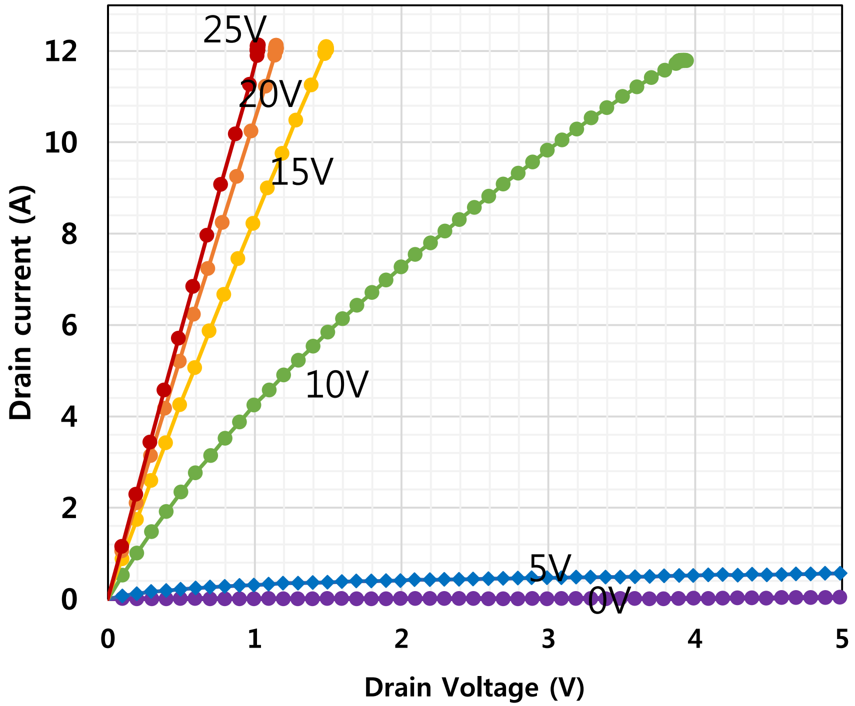
Rsheet (ohm/sq)	Pc (ohm.cm2)
2291.87	4.10E-05

Technical Accomplishments and Progress

- **Lot1 evaluation: nominal structure**

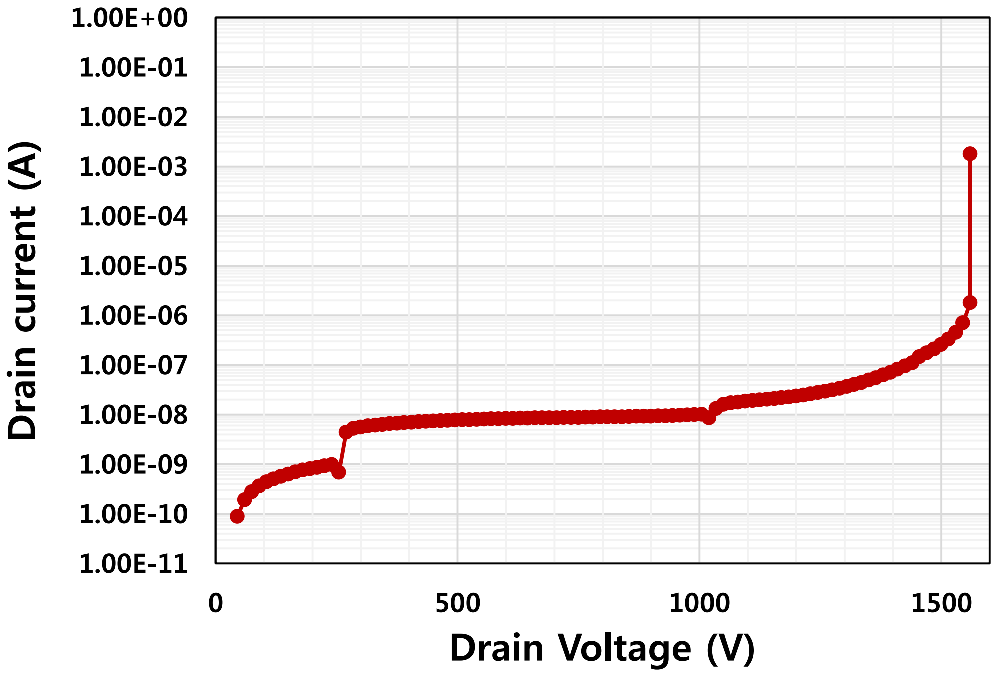
Cell pitch 5.6um, Lch=0.5um
Conv. Pwell (~0.7um)
Deep JFET implant (~0.9um)

Output characteristics



Ron,sp=4.12 mohm-cm2

Forward blocking characteristics



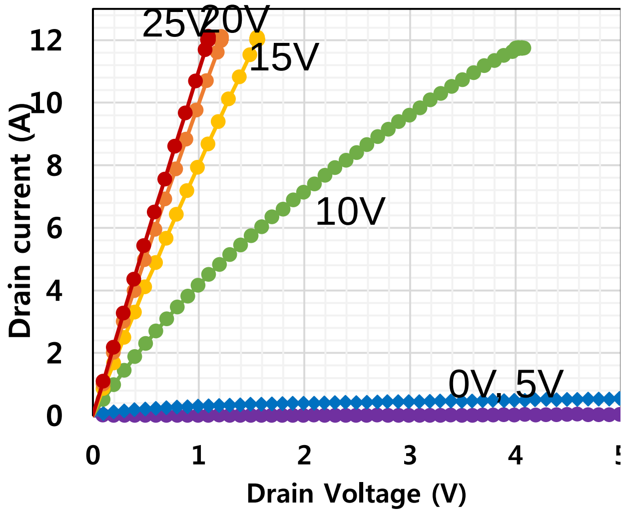
BV=1560V

Technical Accomplishments and Progress

- **Lot1 evaluation: JFET width variations**

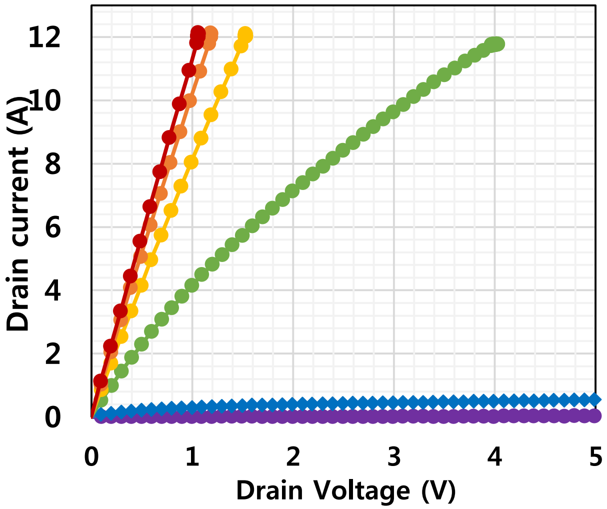
Half JFET
width=0.6um

Ron,sp=4.33 mohm-cm2



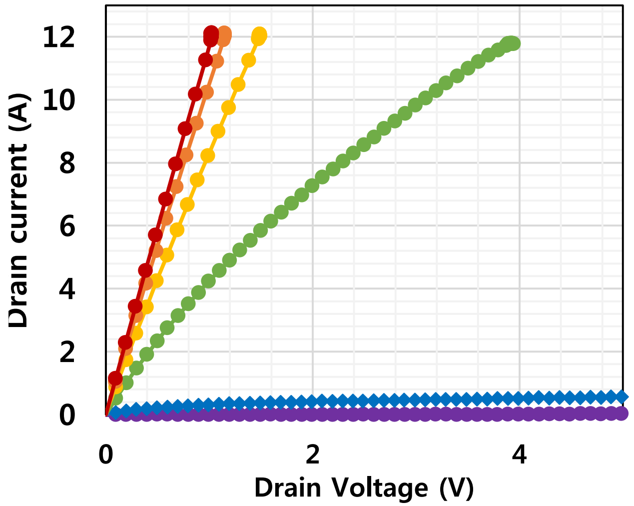
Half JFET
width=0.7um

Ron,sp=4.24mohm-cm2



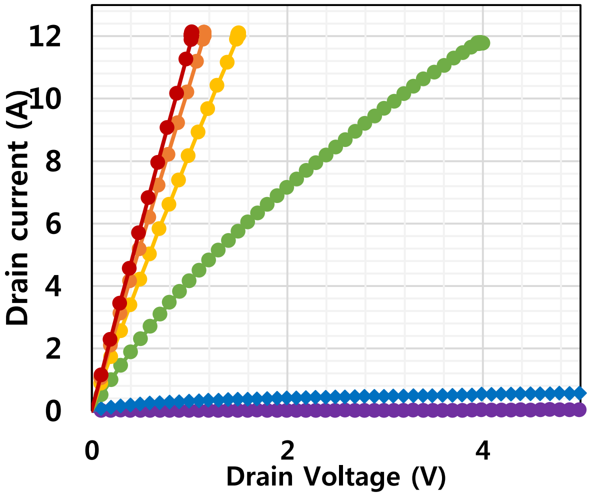
Half JFET
width=0.8um

Ron,sp=4.12mohm-cm2



Half JFET
width=0.9um

Ron,sp=4.09mohm-cm2

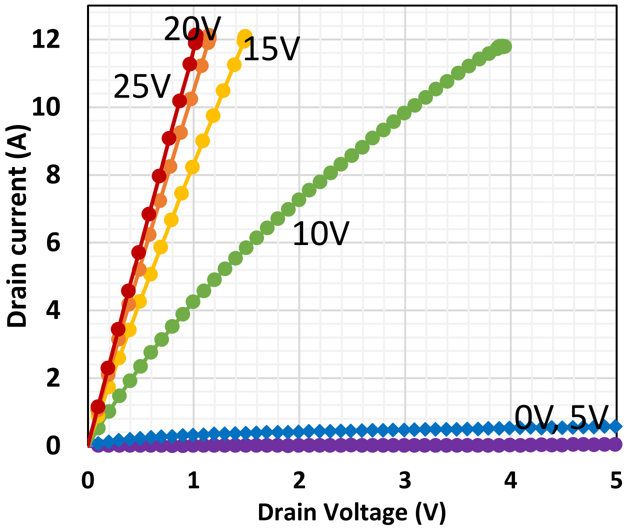


Technical Accomplishments and Progress

- **Lot1 evaluation: channel length variations**

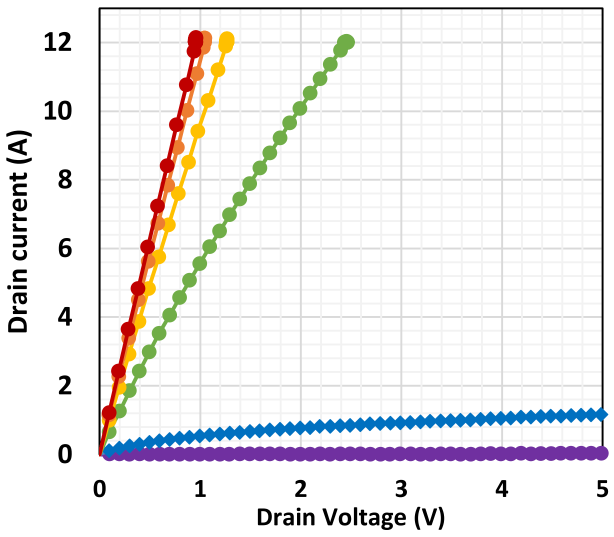
Lch=0.5 um

Ron,sp=4.12mohm-cm2



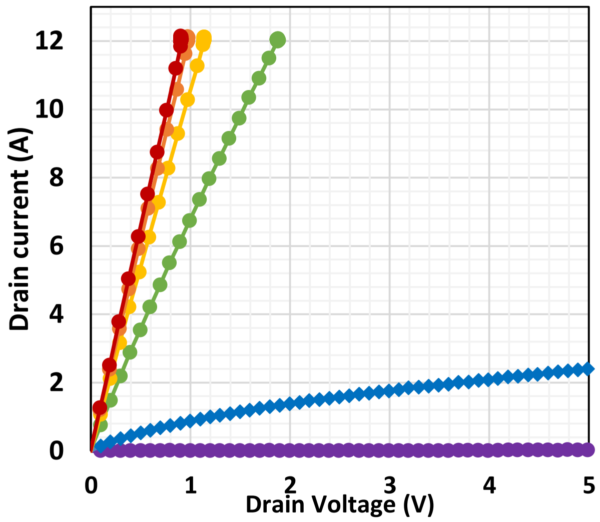
Lch=0.4 um

Ron,sp=3.78mohm-cm2



Lch=0.3 um

Ron,sp=3.56mohm-cm2

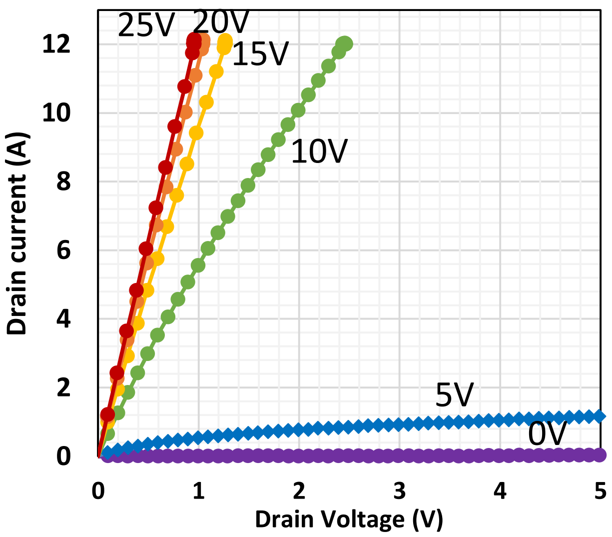


Technical Accomplishments and Progress

- **Lot1 evaluation: cell pitch variations**

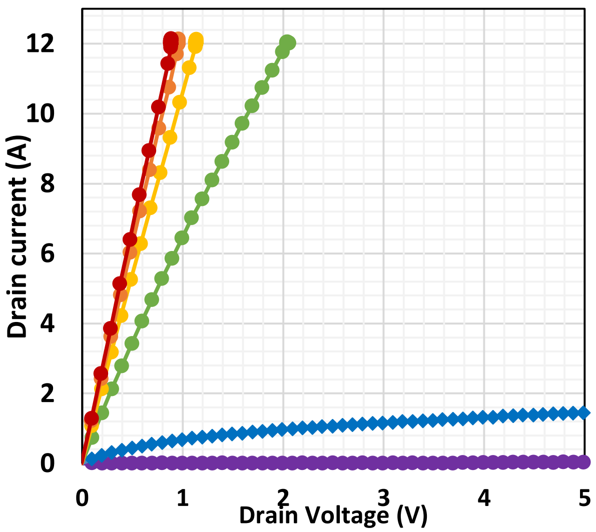
Cell pitch
5.6um

Ron,sp=3.78mohm-cm2



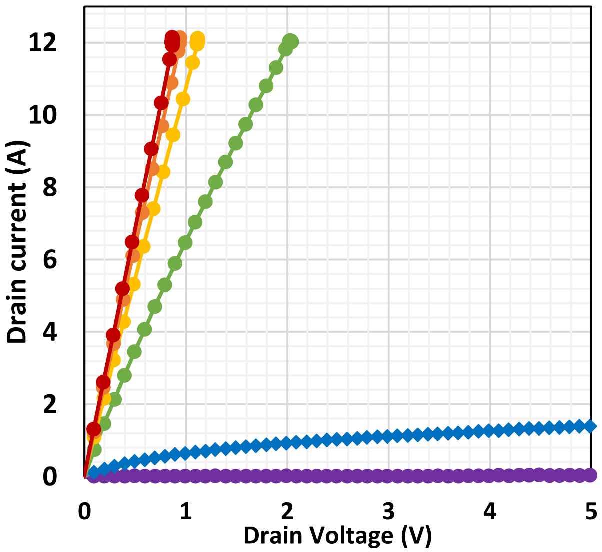
Cell pitch
4.6um

Ron,sp=3.54mohm-cm2



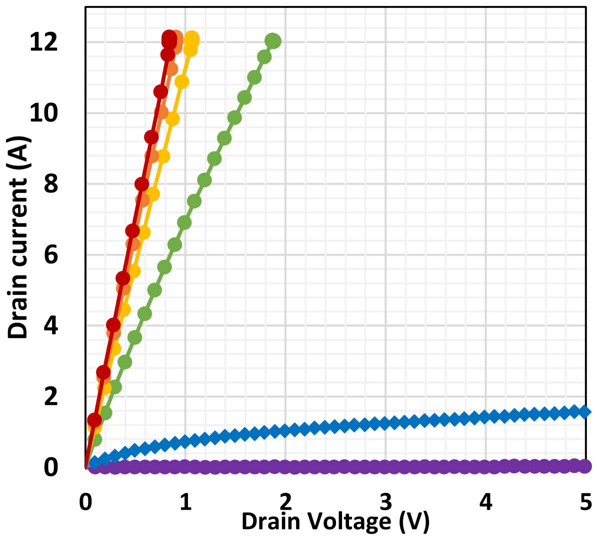
Cell pitch
4.4um

Ron,sp=3.45mohm-cm2



Cell pitch
4.0um

Ron,sp=3.30mohm-cm2



Collaboration and Coordination

	Collaboration	Relationship	Comments
ADI	Multiple projects	Fabrication service	ADI is providing process services for government projects that SUNY Poly leads.
The Ohio State University	Multiple government projects	Partner for EDTC project	OSU will evaluate reliability as well as performances of devices that SUNY fabricated.
Sandia National Laboratories	EDTC	Leading national lab	SNL and team members in EDTC will evaluate devices
ARL / ONR	MUSiC	Funding agency	Currently developing 13kV SiC MOSFETs

Remaining Challenges and Barriers

Fabrication resources

- Multiple resources in U.S. need to be secured.

Process readiness

- Critical processes such as gate oxide formation need to be developed for high channel mobility;

Packaging research

- Advanced packaging research is one of important aspects in reducing the chip cost.

Proposed Future Research

Process development

- Gate oxide process for high mobility and high quality will be developed;
- Channeling implants and room temperature implants will be developed;

Device innovation

- Cell structure and edge termination area will be optimized in terms of performance (static and dynamic) and reliability;

Reliability assessment

- Collaboration with OSU - Feedback on the design of device and process.

Packaging research

- High voltage, high temperature, high performance packaging will be developed.

Summary

Key points

- Development of CPR power devices on SiC is urgently required.
- All aspects (CPR) need to be considered in a comprehensive research program.
- Strong team (fab and partner) was formed to accomplish the proposed goals.
- Gen1 device has been successfully developed.

Relevance

Overall objectives in this project

- The primary objective of this project is to demonstrate highly reliable wide bandgap AlGa N/GaN HEMT power devices.

Technology Summary

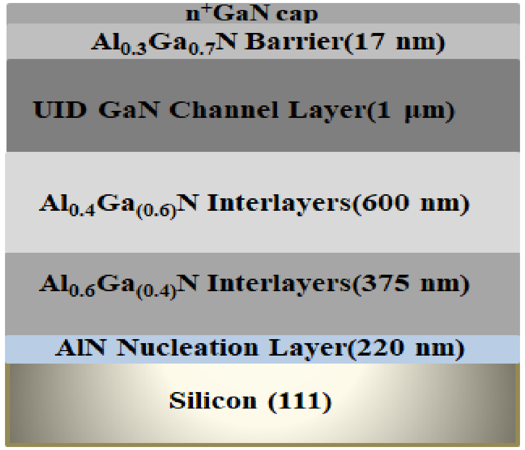
- In this project, we will demonstrate AlGaN/GaN (MIS)HEMT power devices with superior performance and reliability. To accomplish this goal, growth and processing conditions will be optimized for AlGaN/GaN (MIS)HEMT devices on bulk GaN to reduce the effect of defects in the bulk and at interfaces. A detailed comparison to devices on established structures on foreign substrates will be made. As a co mponent of the project, performance and reliability issues of MIS gate are addressed.

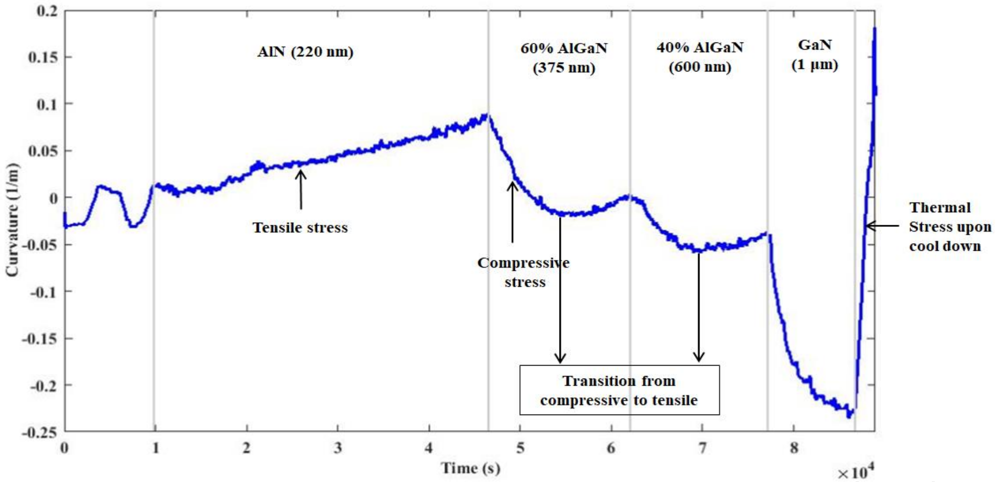
Description of the Technology's Impact

- The increased reliability of AlGaN/GaN HEMT devices will allow for more effective commer -cialization of GaN-based technologies.

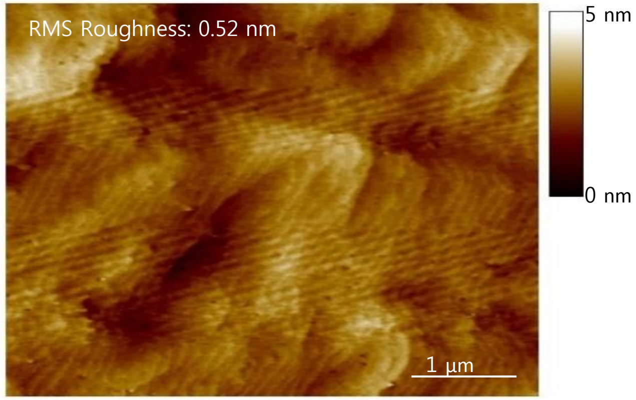
Progress: AlGaN/GaN Growth on (Silicon) Foreign Substrate

- AlGaN/GaN epitaxial growth optimized for foreign substrates (sapphire and silicon)
- GaN grows under tensile strain on Si (17 % lattice mismatch)
- Stress mitigation $Al_xGa_{1-x}N$ layers required for Si substrates to prevent film cracking (due to high TCE mismatch) and improve reliability
- Surface roughness of HEMT-on-Si comparable to Best HEMT-on-sapphire. Atomic step edges more clearly visible on HEMT-on-sapphire, as seen in AFM scans below

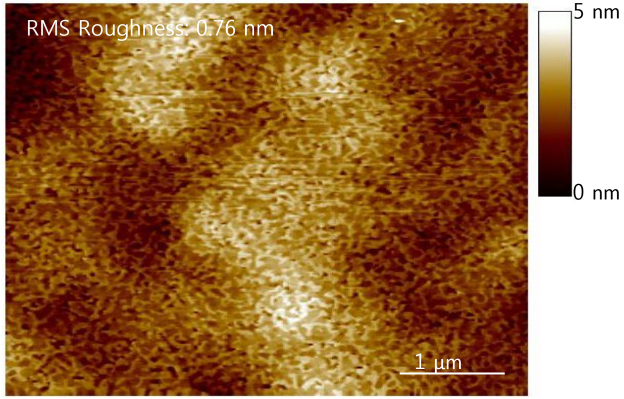




In situ curvature measurement to monitor stress build up during growth. This allows for optimization of stress mitigation interlayer thickness, as well as to insert desirable level of stress in layers.



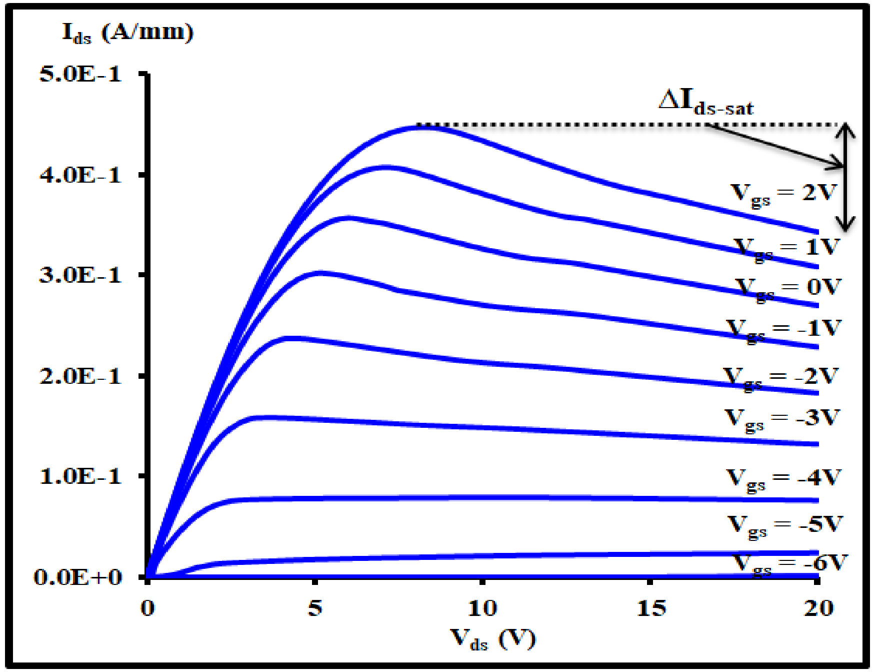
AFM scan of HEMT-on-sapphire



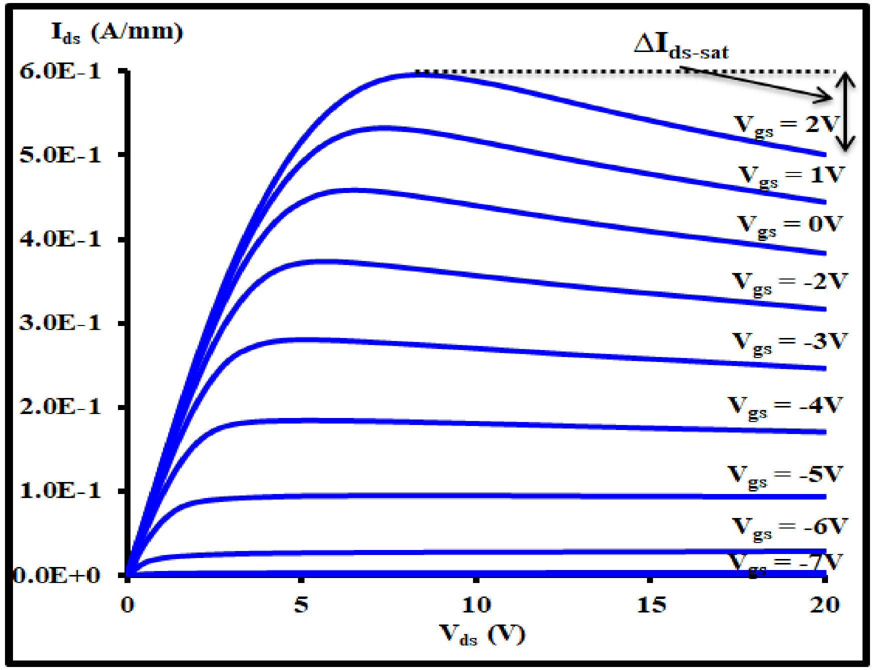
AFM scan of HEMT-on-Si

Progress: Device Characteristics and comparison of HEMT on Si and Sapphire Substrate

HEMT on Sapphire



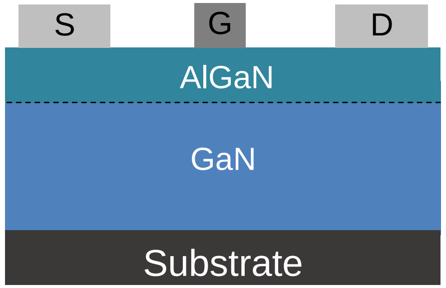
HEMT on Silicon



- Maximum power density 5 W/mm in HEMT on Si, 3.79 W/mm in HEMT on sapphire at V_{ds} = 8.5 V
- Reduction in saturation drain current ($I_{ds\text{-}sat}$) is observed at high power density as V_{ds} is increased due to self-heating effects
- The magnitude of the negative slope is larger in HEMT on sapphire with $\Delta I_{ds\text{-}sat}$ > 100 mA/mm due to poor heat dissipation

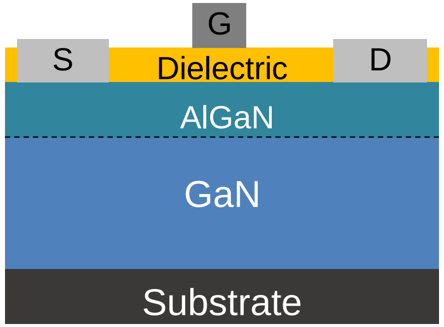
Progress: Performance/Reliability of Gate Dielectric

- Conventional HEMTs use Schottky gate to modulate 2DEG
  - High gate leakage, especially when forward biased
- Gate dielectric used for low leakage, enhancement mode HEMTs
  - High density of interface trapping states (D_{it}) at (Al)GaN/dielectric interface, causes performance and reliability issues
- Al_2O_3 attractive choice for dielectric because it has favorable band offset to GaN and a relatively high dielectric constant

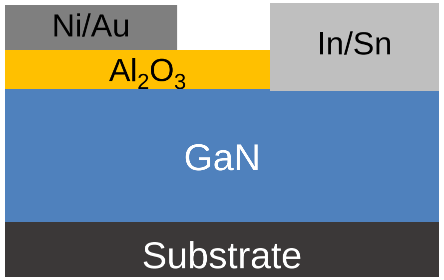


Cross-sectional schematic of Schottky-gated HEMT (not to scale)

- Al_2O_3/GaN MIS capacitor fabricated as separate device to measure characteristics of dielectric
  - Al_2O_3 annealed in forming gas (5%H_2/95%N_2) for range of temperatures and times
- Simplified device with no AlGaN/GaN heterojunction
  - No 2DEG
  - Capacitance determined by one semiconductor layer and dielectric



Cross-sectional schematic of MIS-gated HEMT (not to scale)



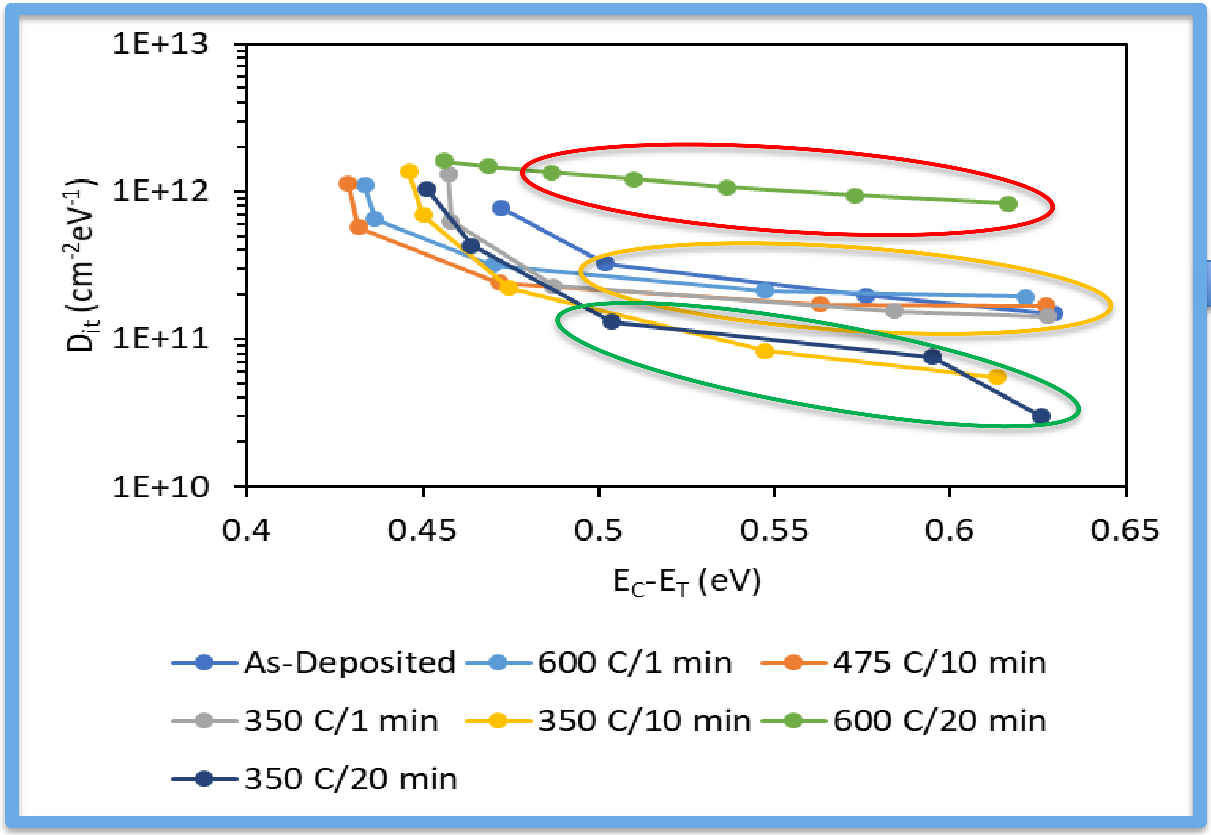
Cross-sectional schematic of Al_2O_3 MIS capacitor with un-optimized ohmic contact (not to scale)

Forming gas annealing conditions applied to Al_2O_3 after deposition

Temp (°C)	1 min	10 min	20 min
600	X		X
475		X	
350	X	X	X

Progress: D_{it} vs E_T

- D_{it} of Al_2O_3/GaN interface extracted for each annealing condition using conductance method
- D_{it} plotted as a function of energy position in band gap
- Low temperature anneal for longer period of time is more beneficial-Higher temperatures cause degradation

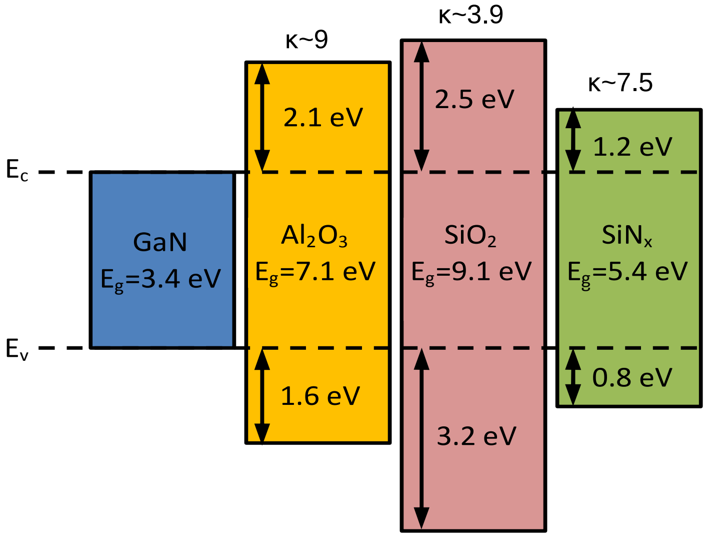


Observations:

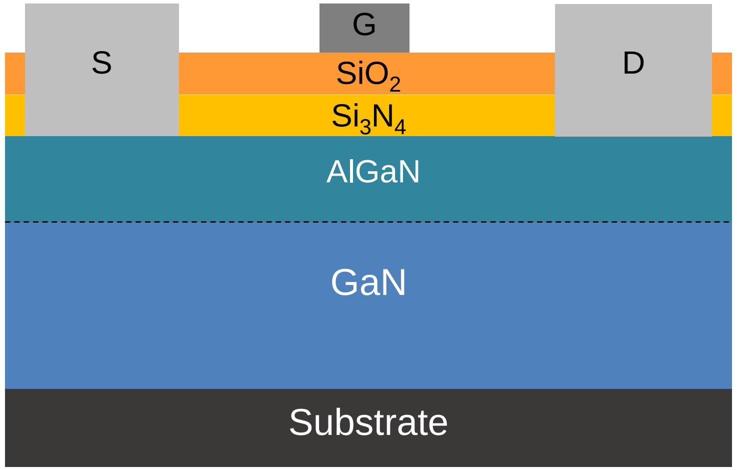
- All devices tend toward ~1-2×10^{12} at shallow levels
- **Three "groups" of trap densities emerge at deeper levels:**
  - High (~1×10^{12}): 600 °C/20 min
  - Medium (~2×10^{11}): As-dep, 350 °C/1 min, 475 °C/10 min, 600 °C/1 min
  - Low (~8×10^{10}): 350 °C/10 min, 350 °C/20 min

Progress: Si_3N_4/SiO_2 MISHEMT Devices

- Al_2O_3 is attractive choice for MISHEMT gate dielectric because it has favorable band offset to GaN and relatively high dielectric constant
- Al_2O_3 degrades at high processing temperatures that is required for HEMT fabrication
- Si_3N_4 and SiO_2 have higher thermal stability than Al_2O_3, but SiO_2 has a relatively low dielectric constant and Si_3N_4 does not have large band offset relative to GaN
- Use of Si_3N_4/SiO_2 bilayer may result in high band offset while maintaining a relatively high dielectric constant
- MISHEMTs are fabricated using ALD Si_3N_4/SiO_2 bilayer where vacuum was not broken between the deposition of each dielectric material

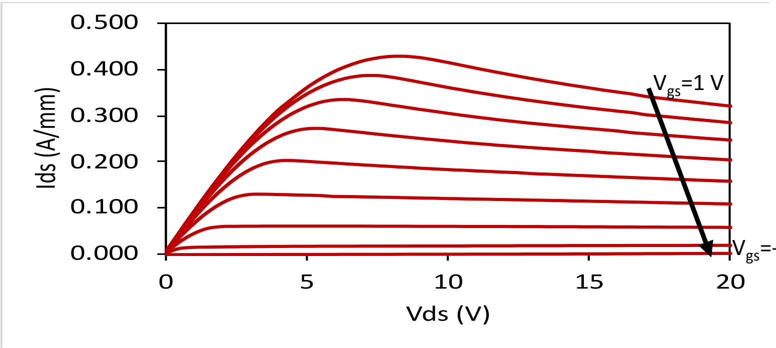


Schematic showing band offsets between GaN and three common dielectric materials: Al_2O_3, SiO_2, and SiN_x

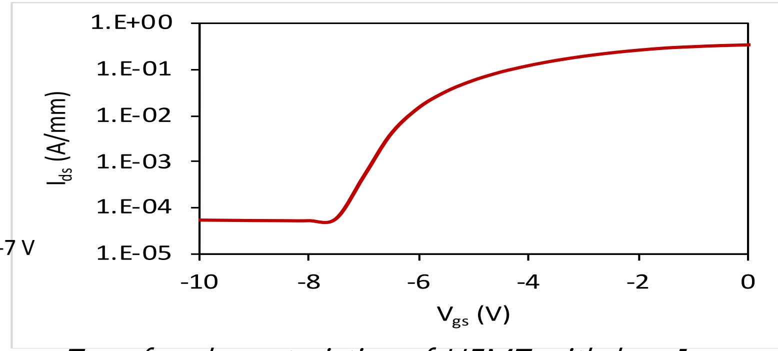


Cross-sectional schematic of Si_3N_4/SiO_2 MISHEMT (not to scale)

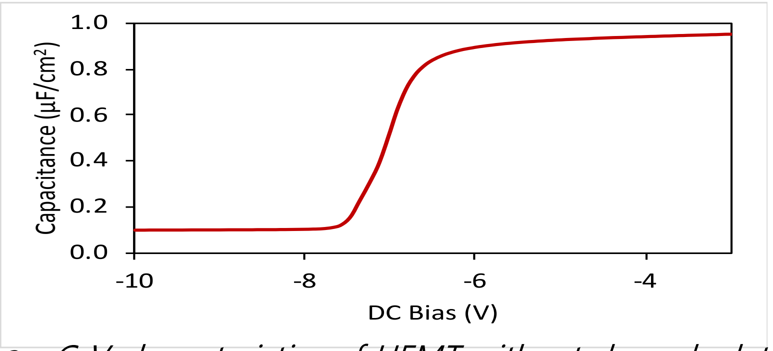
Progress: MISHEMT I-V and C-V Characterization



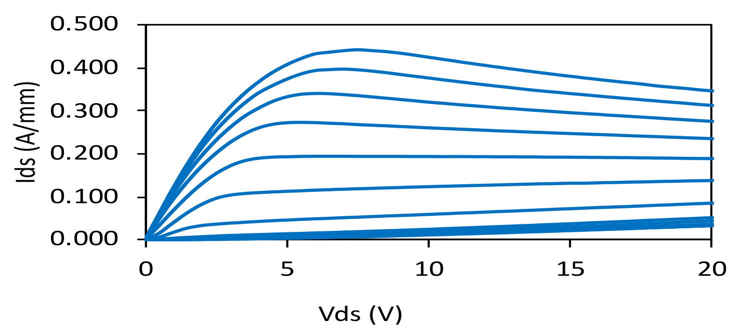
Output characteristics of high quality HEMT with low I_{OFF}



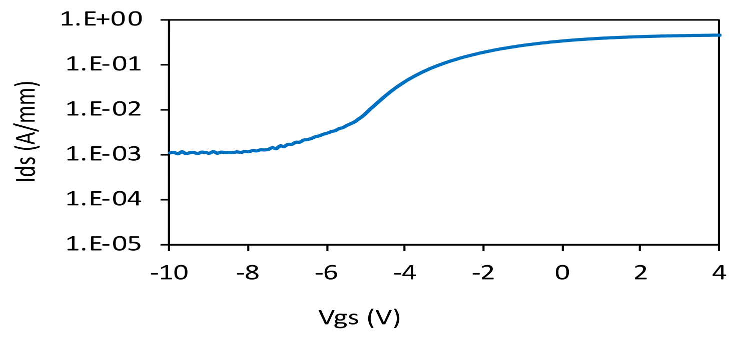
Transfer characteristics of HEMT with low I_{OFF} and abrupt turn on



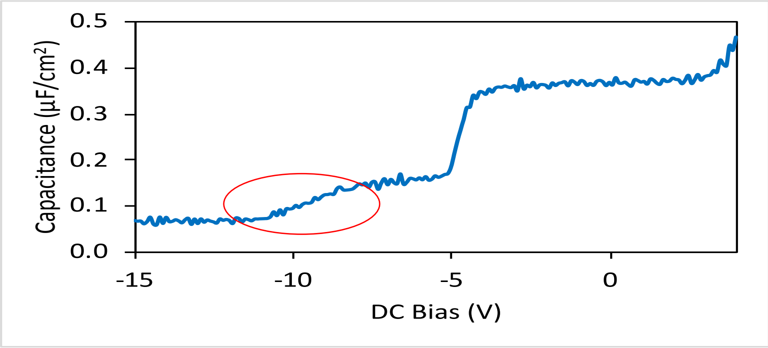
C-V characteristics of HEMT without deep depletion characteristic



Output characteristics of MISHEMT showing relatively high I_{OFF} and sub-threshold gate dependence.



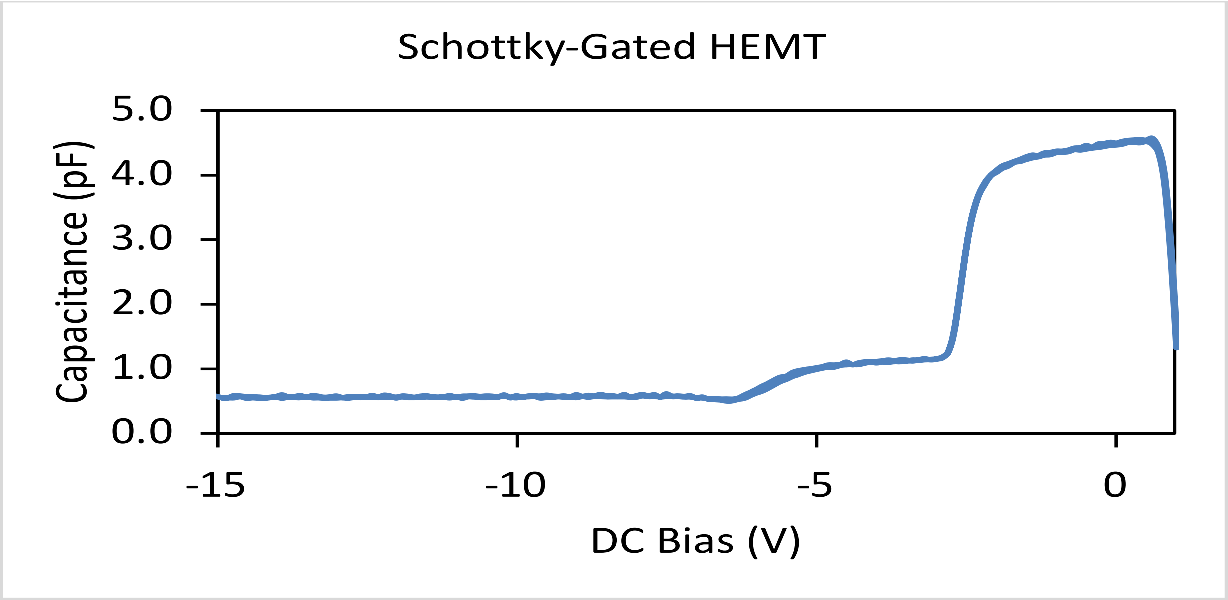
Transfer characteristics of MISHEMT showing high degree of sub-threshold gate dependence.

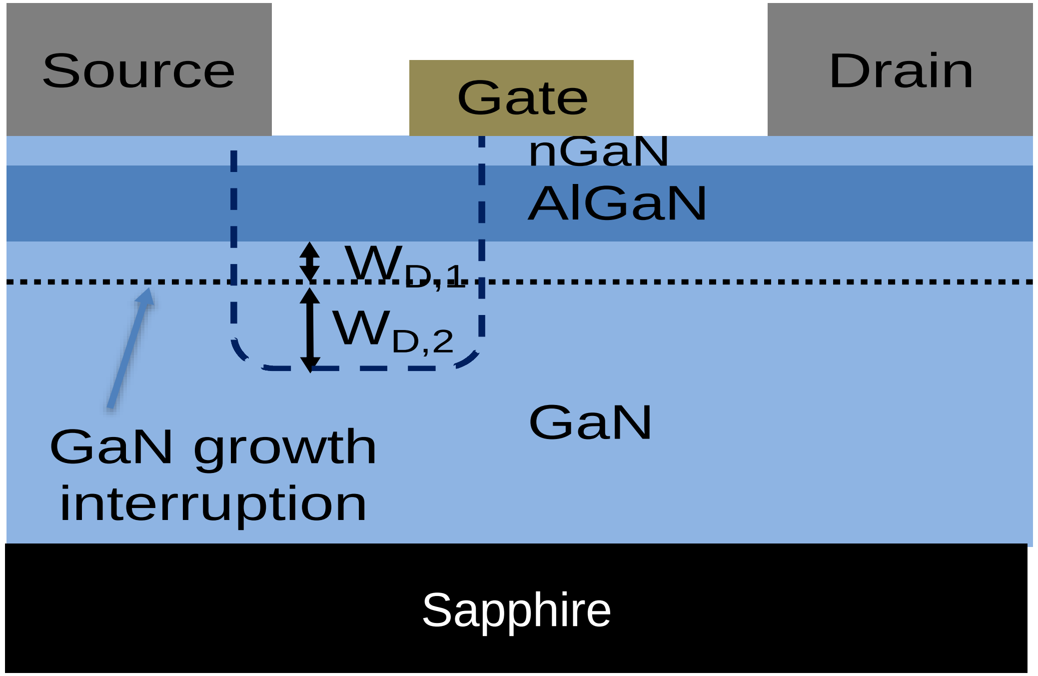


C-V characteristics of MISHEMT with deep depletion at high negative bias circled.

- MISHEMT devices exhibit high I_{OFF} which is modulated by gate bias (bottom), compared to high quality HEMT devices with low I_{OFF} and abrupt turn-on (top)
- Sub-threshold gate dependence appears to be related to a deep depletion at high negative bias (bottom) that is not present in high quality HEMT devices (top)
- It is critical to minimize presence of deep donor states and/or high background doping concentration within GaN buffer-otherwise this may prevent depletion width from extending, resulting in high I_{OFF}

Progress: Origin of Secondary Depletion





- Similar C-V characteristics measured on Schottky-gated HEMT → secondary depletion related to epitaxial layers, not dielectric
- GaN template grown prior to AlGaN growth
  - Before AlGaN growth layer, ~200 nm GaN grown to “bury” the interface
- At the HEMT threshold voltage (-3 V), depletion width is expected to be ~380 nm
- High levels of defects/impurities may pin the depletion width at the regrowth interface, preventing further depletion until a high enough bias is applied
- Higher reliability is expected of HEMTs grown on bulk GaN; buffer layers of high resistivity and higher quality; and no growth interruptions

Technical Progress Summary

- High quality AlGaN/GaN heterostructures grown on Si and sapphire substrates
  - Nucleation layers and stress mitigation layers optimized to reduce lattice misfit stress
  - RMS roughness of HEMT-on-sapphire and HEMT-on-Si similar
- AlGaN/GaN HEMT fabrication and characterization performed
  - High I_{ON}/I_{OFF}
  - Low gate leakage
  - Superior heat dissipation observed in Si substrate
- Progress in growth/fabrication parameters to improve (MIS)HEMT performance and reliability
  - Low temperature anneal in forming gas beneficial to Al_2O_3
  - High temperature processing degrades Al_2O_3
  - Si_3N_4/SiO_2 promising as gate dielectric, can withstand high temperature ohmic metallization and to facilitate an ohmic-first process.
  - Proximity of GaN overgrowth interface to heterointerface found to negatively impact (MIS)HEMT performance
- Successful growth of high quality, thick (>5 micron) GaN on GaN
  - RMS roughness ~1 Å
  - Low background impurity concentration

Collaboration and Coordination

	Collaboration	Relationship	Comments
ARL	Other projects	Funding agency	Developing dielectric (stack) for high quality semiconductor-dielectric interface and high reliability AlGaN/(Al)GaN HEMT

Challenges

- Al_2O_3 requires additional processing considerations to be viable gate dielectric
  - Ohmic metallization requires ~850 °C anneal, Al_2O_3 degrades at high temperatures
  - Al_2O_3 deposition after ohmic metallization results in highly defective interface and poor-quality devices
- Presence of overgrowth interface near heterointerface affects depletion characteristics, contributes to increased I_{OFF}
  - UID GaN overgrowth thickness must be optimized for successful high voltage HEMT-on-GaN implementation

Future Work

- Novel method of surface passivation/protection with *in situ* MOCVD SiN_x cap to preserve high-quality dielectric/semiconductor interface while allowing for ohmic metallization before Al_2O_3 deposition
- Homoepitaxial growth of AlGaN/GaN on bulk GaN substrate and fabrication of HEMTs
- Fabrication of (MIS)HEMT on GaN and performance comparison to determine impact of dislocation defects on reliability